

2.0 W CW X-Band GaInP/GaAs Heterojunction Bipolar Transistor

William Liu, *Member, IEEE*, Tae Kim, *Member, IEEE*, and Ali Khatizbadeh, *Member, IEEE*

Abstract— We report 2.0 W CW (continuous wave) output power at 9.5 GHz with a GaInP/GaAs HBT having a total emitter area of $2 \times 500 \mu\text{m}^2$. The collector-emitter bias dependence and the frequency dependence of the large-signal performance of both the 2×400 and $2 \times 500 \mu\text{m}^2$ unit cells are described. The uniformity of the output power and power-added efficiency is also discussed.

THERE are several advantages to replacing AlGaAs by GaInP as the emitter material of GaAs-based heterojunction bipolar transistors (HBT's) [1–3]. To date, GaInP/GaAs HBT's have demonstrated near-ideal current-voltage characteristics [4], high-current gain exceeding 1,000 [5], [6] small offset voltage of 36 mV [7], excellent surface passivation of the extrinsic base surface [6], constant current gain in the temperature range between 25 °C and 300 °C [8], and maximum oscillation frequencies exceeding 100 GHz [9], [10]. These reports establish GaInP/GaAs HBT's as a potential alternative to the more conventional AlGaAs/GaAs HBT's.

GaInP/GaAs HBT's also received considerable interest for power applications. The first large-signal power study of GaInP/GaAs HBT's reported 1W CW power at X-band (10 GHz) [11]. Other large-signal power results were obtained at 3 and 12 GHz [12], [13]. These results, though encouraging, are preliminary and often measured from only one or few transistors of the fabricated wafer. In this study, we attempt a more in-depth characterization of the power performance. Several transistors were measured to establish the uniformity of the fabricated GaInP/GaAs HBT wafer. The measured frequencies range from 8, 8.5, 9, 9.5 to 10 GHz and the collector bias varied from 10, 12, to 13 V. Transistors with two different sizes are fabricated. From a transistor having a total emitter area of $2 \times 500 \mu\text{m}^2$, we obtained 2.0 W (4.0 W/mm) CW output power at 9.5 GHz, representing a two-fold improvement over the previously reported large-signal power at X-band [11].

The wafer was grown by metalorganic chemical vapor deposition (MOCVD) using tertiarybutylarsine [14]. The n-type and p-type dopants were disilane and carbon tetrachloride, respectively. The epitaxial structure consists of a 2000 Å n-GaAs cap layer doped at $5 \times 10^{18} \text{ cm}^{-3}$, an 1000 Å n-GaInP active emitter layer doped at $2 \times 10^{17} \text{ cm}^{-3}$, an 800 Å p-GaAs base layer doped at $3 \times 10^{19} \text{ cm}^{-3}$, an 1 μm n-GaAs

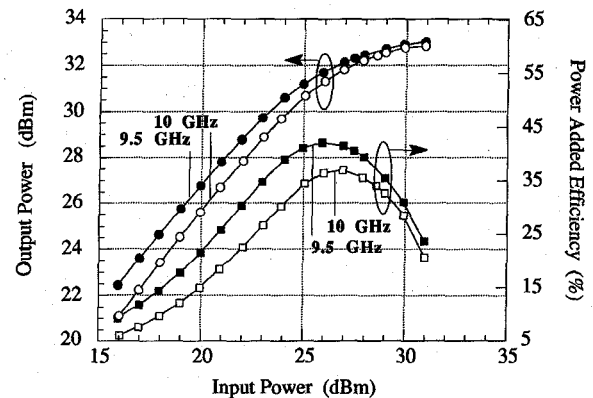


Fig. 1 Measured large-signal output power and power-added efficiency as a function of the r.f. input power for a $2 \times 500 \mu\text{m}^2$ device. The measurements were done at 9.5 and 10 GHz. The collector bias was 12 V.

collector layer doped at $1 \times 10^{16} \text{ cm}^{-3}$, and an 1 μm n-GaAs subcollector doped at $3 \times 10^{18} \text{ cm}^{-3}$. The fabrication process resulting in self-aligned base-emitter contacts is identical to that previously reported [10], [11]. The wafers were lapped to a 4-mil thickness and the emitter pads were grounded to the Au-plated backside.

The small-signal measurement made on a two-finger device ($2 \times 60 \mu\text{m}^2$) demonstrated a cut-off frequency (f_T) of 27 GHz and a maximum oscillation frequency (f_{max}) of 90 GHz when operated at a collector-emitter bias (V_c) of 4 V and a collector current of 21 mA. The small-signal power gain is ~ 17 dB at 10 GHz. All large-signal measurements were performed with class AB operation. That is, the DC base-emitter voltage was chosen to bias the transistor in the nearly-on position. Only a small addition of the r.f. input bias is required to fully turn on the transistor. The layout and a scanning electron microscope (SEM) image of these unit-cells have been illustrated [11], [15]. The transistors were tuned with external tuners having a 15:1 VSWR tuning range. Tuning chip capacitors were used to provide better input impedance matching. Since the input tuner was tuned near the extreme of the tuning range, we expect about 0.5 to 1 dB of power loss which is not accounted for. Therefore, the reported results represent conservative figures.

Fig. 1 illustrates the measured large-signal output power (P_{out}) and power-added efficiency (PAE) as a function of the r.f. input power (P_{in}) for a $2 \times 500 \mu\text{m}^2$ device. The measurements were performed at 9.5 and 10 GHz, both at a collector bias of $V_c = 12$ V. The collector current increases from 124 mA at $P_{in} = 16$ dBm to 250 mA at $P_{in} = 28.6$

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The authors are with Central Research Laboratories, Texas Instruments, Dallas, TX 75265.

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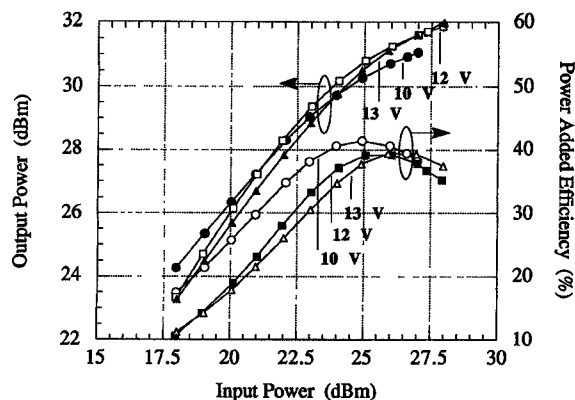


Fig. 2 Measured large-signal output power and power added efficiency as a function of the r.f. input power for a $2 \times 400 \mu\text{m}^2$ device. The measurements were done with the collector bias varying from 10, 12 to 13 V, and the operating frequency was 10 GHz.

dBm, indicating a class AB operation. As shown, the largest output power measured was 2.0 W (33.01 dBm) and 1.92 W (32.83 dBm) at 9.5 and 10 GHz, respectively. The 2.0 W result corresponds to a power density of 4.0 W/mm. This value, though impressive, is not near the estimated theoretical limit of 8.5 W/mm [16], indicating that further improvement in the device performance is possible. The linear power gains at such power output levels are 6.82 and 5.83 dB at 9.5 and 10 GHz, respectively. The drastic difference in the power gains reflects the fact that no pre-matching circuit was used in the measurement and that additional loss in input impedance matching occurred at higher frequencies. Also note that the large-signal gain of ~ 6 dB is significantly smaller than the small-signal gain of ~ 17 dB at 10 GHz. This results because both V_c and I_c vary significantly during a large-signal testing. The quoted small-signal gain represents only a single value obtained at a fixed bias condition. It does not exemplify the gains achievable at the other bias conditions encountered during a large-signal bias swing.

Fig. 2 shows the measured P_{out} and PAE as a function of P_{in} for a $2 \times 400 \mu\text{m}^2$ device. All measurements were done at 10 GHz, but V_c varies from 10, 12, to 13 V. At lower P_{in} levels, the linear power gain is about 6.3 dB for $V_c = 10$ and 12 V, but decreases by 0.5 dB at $V_c = 13$ V. The PAE is also the highest for $V_c = 10$ V, reaching 41.4 %, whereas for $V_c = 12$ and 13 V, the PAE is about 5–7 % lower. However, larger P_{out} levels are achieved with higher-collector bias voltages at 2-dB compression points. P_{out} 's are 30.92, 31.71, and 32.3 dBm for $V_c = 10, 12$, and 13 V, respectively. (The 32.3 dBm power corresponds to a 4.24 W/mm power density.) Therefore, though higher PAE is obtained at the 10 V bias, larger P_{out} is achieved with higher biases. Since P_{out} improvement from $V_c = 12$ to 13 V is marginal, the rest of the measurements are done with $V_c = 12$ V.

Fig. 3 illustrates the frequency dependence of the device performance for another $2 \times 400 \mu\text{m}^2$ device. The plotted results are the values at the 2-dB compression points. Fig. 3 demonstrates that P_{out} is relatively the same throughout the frequency range, varying from 32.05, 32.0, 31.84, 31.99 to 31.64 dBm as the frequency increases from 8, 8.5, 9, 9.5 to

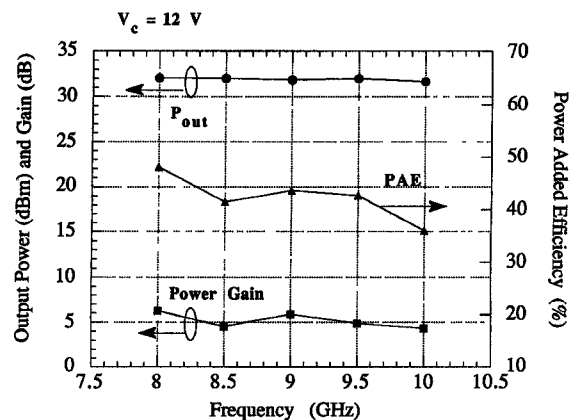


Fig. 3 Measured frequency dependence of the large-signal performance for another $2 \times 400 \mu\text{m}^2$ device at 2-dB compression points. The collector bias was 12 V, and the frequency varies from 8, 8.5, 9, 9.5 to 10 GHz.

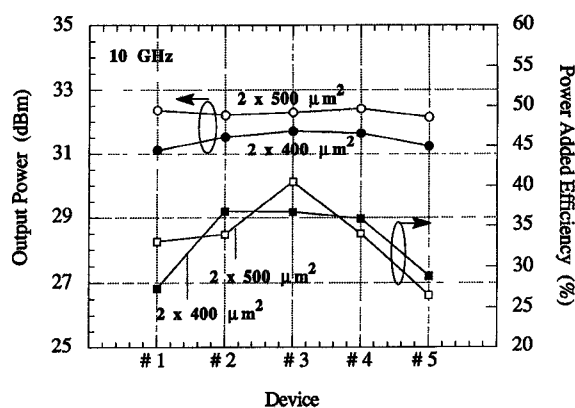


Fig. 4 Measured output power and power-added efficiency at 2-dB compression points of various $2 \times 400 \mu\text{m}^2$ and $2 \times 500 \mu\text{m}^2$ devices. The frequency was 10 GHz and the collector bias was 12 V.

10 GHz. Similarly, the power gain varies from 6.26, 4.51, 5.87, 4.87 to 4.29 dB in this frequency range. The PAE reveals a more noticeable feature, decreasing from 48, 41.4, 43.6, 42.6 to 35.9 % as the frequency increases.

The uniformity of the fabricated piece (half-piece) of wafer is also examined. Fig. 4 demonstrates the measured P_{out} and PAE at 2-dB compression points of various $2 \times 400 \mu\text{m}^2$ and $2 \times 500 \mu\text{m}^2$ devices. These devices, a total of five for transistors of each size, were sampled across the entire half-piece of the fabricated wafer. As shown, some variation of device performance is observed across the wafer, with the averages of P_{out} varying from 1.40 to 1.69 W for the 2×500 and $2 \times 400 \mu\text{m}^2$ unit-cells, respectively. The standard deviations are 0.08 and 0.04 W, respectively. The PAE, in contrast, displays more variation for both unit-cells. The average PAEs are 33.1 and 33.58 %, respectively, and the standard deviations are 4.6% and 5.0%, respectively.

In summary, a more in-depth characterization of GaInP/GaAs HBT's than the previously reported one was performed. A 2.0 W CW output power was achieved for a $2 \times 500 \mu\text{m}^2$ device at 9.5 GHz. The collector bias and the frequency dependences of the large-signal performance of $2 \times 400 \mu\text{m}^2$ devices were examined. The uniformity of the

large-signal performance in the devices of both sizes was also discussed. The intermodulation distortion (IMD) performance of these GaInP/GaAs HBT's will be tested shortly.

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